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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,150	09/17/2003	Mitsuyoshi Endo	04173.0437	4196

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EXAMINER

NGUYEN, DAO H

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/664,150

Applicant(s)

ENDO ET AL.

Examiner

Dao H. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 and 14-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 and 14-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 September 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This Office Action is in response to the communications dated 09/15/2005.  
Claim(s) 1-12 and 14-16 are active in this application.  
New claim(s) 14-16 have been added.  
Claim 13 has been cancelled.

### **Claim Objections**

2. The claim is objected to for the following reason: In claim 15, lines 1-3, a comma -- , -- should be placed between the phrases "in each of the plurality of semiconductor device portion units" and "each of the pads of said semiconductor chip" for clarity.  
Appropriate correction is required.

### **Remarks**

3. Applicant's arguments filed 09/15/2005 have been fully considered but they are not persuasive.

First, Applicant's argument that the passive element(s) of Admitted Prior Art (APA) and/or of Rahim is/are not semiconductor chip. This argument is not persuasive because passive elements such as capacitors and inductors are well known chips in the art, and they are well known to be formed by various materials, including

semiconductor. Examples of such well known semiconductor chips are in U.S. Patent No. 4,670,770 to Tai, col. 6, lines 3-4; or in U.S. Patent Application Publication No. 2003/0146463 by Klee et al., paragraph [0011]. Alternately, col. 1, line 61 to col. 2, line 6; col. 2, lines 45-61; and col. 6, lines 14-38 of Rahim teach that a passive element such as an inductor can be formed within a silicon-based IC. Therefore, it is clearly that the second chip of APA and/or Rahim is/are semiconductor chip(s).

Second, the argument that the passive element(s) of Admitted Prior Art (APA) and/or of Rahim is/are not provided at a position facing a side of the (first) semiconductor chip is not found persuasive because:

a. As shown in fig. 21A of APA, passive elements 305 are provided on both sides of the semiconductor chip 302. It is clearly that these passive elements 305 are facing the side(s) of the semiconductor chip 302.

b. Similarly, figs. 9-10, and/or col. 5, lines 37-40, col. 6, lines 38-53 of Rahim teach that the passive element 26 is positioned on a side of the semiconductor chip 90. Clearly, the passive element does face the side of the semiconductor chip.

For the above reasons, the rejection in the last Office Action is believed to be proper and retained, and rewritten below to include rejections regarding newly added claims 14-16.

#### **Claim Rejections - 35 USC § 102**

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim(s) 1 and 11 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by admitted prior art (Admission).

Regarding claim 1, Admission discloses a semiconductor device, as shown in figs. 21-22 of the pending application, comprising:

a wiring board 301;

a semiconductor chip 302 provided on said wiring board 301 and having a pad 303 electrically connected to a wiring on said wiring board 301; and

a second semiconductor chip 305 provided on said wiring board 301 at a position facing a side of said semiconductor chip 302, having passive elements integrated therein, and having pads for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to the wiring on said wiring board electrically connected to the pad of said semiconductor chip.

Regarding claim 11, Admission discloses a semiconductor package member, as shown in figs. 21-22 of the pending application, comprising:

a wiring board 301 on which a semiconductor chip 302 is mountable; and

an auxiliary semiconductor chip 305 provided on said wiring board 301 at a position facing a side of said semiconductor chip 302 to be mounted, having passive elements integrated therein, and having pads for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to a wiring on said wiring board.

6. Claim(s) 1-12, and 14-16 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,362,525 to Rahim.

Regarding claim 1, Rahim discloses a semiconductor device, as shown in figs. - 10, comprising:

a wiring board 92 (fig. 9) or 104 (fig. 10);

a semiconductor chip 90 provided on said wiring board and having a pad electrically connected to a wiring on said wiring board 92/104; and

a second semiconductor chip 26 or 98 provided on said wiring board 92/104 at a position facing a side of said semiconductor chip 90, having passive elements integrated therein, and having pads 34 for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to the wiring 30, 32 on said wiring board 92/104 electrically connected to the pad 48 of said semiconductor chip 90.

See further col. 11, line 18 to col. 12, line 34. Note also that the passive element itself is also chip.

Regarding claim 2, Rahim discloses the semiconductor device wherein the passive elements integrated in said second semiconductor chip are elements of one kind, or two kinds or more selected from a group of a capacitor, a resistor, and an inductor. See col. 1, lines 39-40, and col. 11, line 18 to col. 12, line 34.

Regarding claim 3, Rahim discloses a semiconductor device wherein said semiconductor chip 90 is flip-chip-connected to said wiring board 92/104 so as to electrically connect the pad to the wiring on said wiring board. See figs. 9-10. and col. 9, lines 41-65.

Regarding claim 4, Rahim discloses a semiconductor device wherein said semiconductor chip 90 has bonding wire connection to the wiring of said wiring board so as to electrically connect the pad to the wiring on said wiring board. See col. 9, lines 47-58.

Regarding claim 5, Rahim disclose a semiconductor device wherein said second semiconductor chip is flipchip-connected to said wiring board so as to electrically connect the pads for external connection to the wiring on said wiring board. See figs. 9-10.

Regarding claim 6, Rahim discloses a emiconductor device wherein said second semiconductor chip has bonding wire connection to the wiring of said wiring

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board so as to electrically connect the pads for external connection to the wiring on said wiring board. See col. 2, line 62 to col. 3, line 6; col. 9, lines 41-65; and col. 12, lines 14-34.

Regarding claim 7, Rahim discloses a semiconductor device wherein said semiconductor chip and said second semiconductor chip are both 60  $\mu\text{m}$  or less in thickness. This is well known in the art. See also col. 2, lines 7-61.

Regarding claim 8, Rahim discloses a semiconductor device wherein said second semiconductor chip has, besides the pads for external connection used for the flipchip connection to said wiring board, a pad for external connection not contributing to the flipchip connection to said wiring board. See col. 11, line 18 to col. 12, line 33.

Regarding claim 9, Rahim discloses a semiconductor device, as shown in figs. 3-10, comprising:

a plurality of semiconductor device portion units arranged in a lamination direction and each including:

a wiring board 92/104 (figs. 9-10);

a semiconductor chip 90 provided on said wiring board and having a pad electrically connected to a wiring on said wiring board 90; and

a second semiconductor chip 26 or 98 provided on said wiring board 92/104 at a position facing a side of said semiconductor chip 90, having passive elements integrated



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therein, and having pads 34 for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to the wiring 32 on said wiring board 92/104 electrically connected to the pad of said semiconductor chip 90; and

a vertical wiring portion 30 passing through said wiring boards 92/104 of said plural semiconductor device portion units and electrically connecting said wiring boards 92-104 to one another.

See further 7, line 55 to col. 8, line 22; col. 11, line 18 to col. 12, line 34. Note also that the passive element itself is also chip.

Regarding claim 10, Rahim discloses a semiconductor device wherein the passive elements integrated in said second semiconductor chips of the respective plural semiconductor device portion units are elements of one kind, or two kinds or more selected from a group of a capacitor, a resistor, and an inductor. See col. 1, lines 39-40, and col. 11, line 18 to col. 12, line 34.

Regarding claim 11, Rahim discloses a semiconductor package member, as shown in figs. 3-10, comprising:

a wiring board 92/104 (figs. 9-10) on which a semiconductor chip 90 is mountable; and

an auxiliary semiconductor chip 26 or 98 provided on said wiring board 92/104 at a position facing a side of said semiconductor chip to be mounted, having passive

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elements integrated therein, and having pads for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to a wiring 32 on said wiring board 92/104.

See further 7, line 55 to col. 8, line 22; col. 11, line 18 to col. 12, line 34. Note also that the passive element itself is also chip.

Regarding claim 12, Rahim discloses a semiconductor package member wherein the passive elements integrated in said auxiliary semiconductor chips are elements of one kind, or two kinds or more selected from a group of a capacitor, a resistor, and an inductor. See col. 1, lines 39-40, and col. 11, line 18 to col. 12, line 34.

Regarding claim 14, Rahim discloses a semiconductor device wherein each of the pads of said second semiconductor chip electrically connected to the pad of said semiconductor chip is positioned to be adjacent to said pad of said semiconductor chip. See figs. 3-10.

Regarding claim 15, Rahim discloses a semiconductor device wherein in each of the plurality of semiconductor device portion units each of the pads of said second semiconductor chip electrically connected to the pad of said semiconductor chip is positioned to be adjacent to said pad of said semiconductor chip. See figs. 3-10.

Regarding claim 16, Rahim discloses a semiconductor package member wherein each of the pads of said auxiliary semiconductor chip electrically connected to the wiring on said wiring board is positioned to be adjacent to a pad of said semiconductor chip to be mounted, the pad being to be connected to said wiring. See figs. 3-10.

### **Conclusion**

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

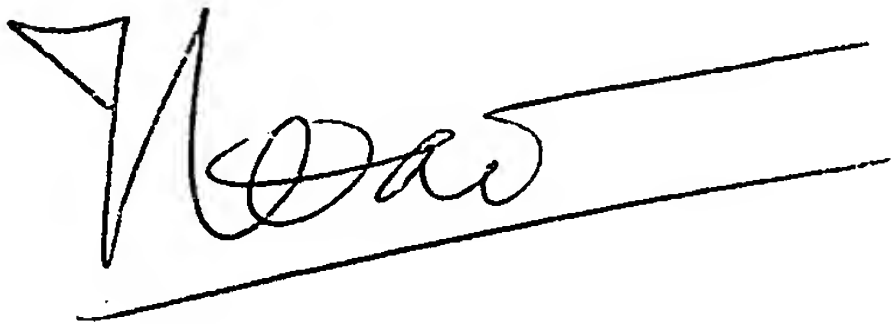
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's

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supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all Customer Service is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

A handwritten signature in black ink, appearing to read 'Dao H. Nguyen', written over two horizontal lines.

Dao H. Nguyen  
Art Unit 2818  
November 15, 2005

A handwritten signature in black ink, appearing to read 'David Nelms', written over two horizontal lines.

David Nelms  
Supervisory Patent Examiner  
Technology Center 2800